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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,217	09/16/2003	Ping Hsu	NTCP0021USA	2216

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NAIPO (NORTH AMERICA INTERNATIONAL PATENT OFFICE)
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MERRIFIELD, VA 22116

EXAMINER	
PERKINS, PAMELA E	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 02/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,217	HSU ET AL.	
	Examiner	Art Unit	
	Pamela E Perkins	2822	

-- The MAILING DATE of this communication appears on the cover she t with the correspond nc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This office action is in response to the filing of the application papers on 16 September 2003. Claims 1-8 are pending.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: 37; see figure 4. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wong et al. (6,436,760) in view of Shen (6,472,702).

Wong et al. disclose a method for fabricating a trench capacitor where a silicon substrate is etched to form a deep trench (1); doping the deep trench (1) to form a buried diffusion plate (5) in the substrate at a lower portion of the deep trench (1); lining

the deep trench with a node dielectric layer (6); performing a first polysilicon deposition and recess etching to embed a first polysilicon (Poly1) layer (7) on the node dielectric layer (6) at the lower portion of the deep trench (1), and the Poly1 layer (7) having a top surface, wherein the top surface of the first polysilicon layer (7) and sidewall of the deep trench (1) define a first recess; forming a collar oxide layer (8) on sidewall of the first recess; performing a second polysilicon deposition and recess etching to embed a second polysilicon (Poly2) layer (11) on the Poly1 layer (7); forming a mask layer partially masking the collar oxide layer (8); removing the collar oxide layer (8) not masked by the mask layer and the Poly2 layer (11); removing the mask layer (Fig. 13-14; col. 6, lines 41-55); and performing a third polysilicon deposition and recess etching to embed a third polysilicon (Poly3) layer (14) on the Poly2 layer (11). Wong et al. further disclose doping the deep trench (1) to form a buried diffusion plate (5) in the substrate involves the use of an arsenic silicate glass (ASG) film (2) (col. 5, line 18 thru col. 7, line 51). Wong et al. do not disclose a pad layer formed on the silicon substrate and the node dielectric as an oxide-nitride-oxide (ONO) dielectric layer.

Shen discloses a method for fabricating a trench capacitor where a pad layer (110) is formed on a silicon substrate (100); etching the pad layer (110) and the silicon substrate (100) to form a deep trench; doping the deep trench to form a buried diffusion plate (150) in the substrate (100) at a lower portion of the deep trench; lining the deep trench with a node dielectric layer (160); performing a first polysilicon deposition and recess etching to embed a first polysilicon (Poly1) layer (170) on the node dielectric layer (160) at the lower portion of the deep trench. Shen further discloses doping the

deep trench to form a buried diffusion plate (150) in the substrate involves the use of an arsenic silicate glass (ASG) film (140). Shen also discloses the node dielectric (160) is an oxide-nitride-oxide (ONO) dielectric layer (col. 4, line 3 thru col. 5, line 14).

Since Wong et al. and Shen are both from the same field of endeavor, a method for fabricating a trench capacitor, the purpose disclosed by Shen would have been recognized in the pertinent art of Wong et al. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Wong et al. by a pad layer formed on the silicon substrate and the node dielectric as an ONO dielectric layer as taught by Shen to improve the connection between the capacitor and the active region (col. 2,lines 22-27).

Referring to claim 3, Wong et al. disclose the deep trench of claim 1 wherein the depth is 6 microns below the surface of the substrate (col. 5, lines 18-29). It is noted that the specification contains no disclosure of either the critical nature of the claimed concentrations or any unexpected results arising there from. It would have been obvious to one of ordinary skill in the art for the depth of the deep trench to larger than 6 microns below the surface of the substrate since it has been held that "In such an situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) See MPEP § 2144.05.

Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wong et al. in view of Shen as applied to claims 1-5 above, and further in view of Gonzalez (5,198,386).

Wong et al. disclose a method for fabricating a capacitor device where a silicon substrate is etched to form a deep trench (1); doping the deep trench (1) to form a buried diffusion plate (5) in the substrate at a lower portion of the deep trench (1); lining the deep trench with a node dielectric layer (6); performing a first polysilicon deposition and recess etching to embed a first polysilicon (Poly1) layer (7) on the node dielectric layer (6) at the lower portion of the deep trench (1), and the Poly1 layer (7) having a top surface, wherein the top surface of the first polysilicon layer (7) and sidewall of the deep trench (1) define a first recess; forming a collar oxide layer (8) on sidewall of the first recess; performing a second polysilicon deposition and recess etching to embed a second polysilicon (Poly2) layer (11) on the Poly1 layer (7); forming a mask layer partially masking the collar oxide layer (8); removing the collar oxide layer (8) not masked by the mask layer and the Poly2 layer (11); removing the mask layer (Fig. 13-14; col. 6, lines 41-55); and performing a third polysilicon deposition and recess etching to embed a third polysilicon (Poly3) layer (14) on the Poly2 layer (11). Wong et al. further disclose doping the deep trench (1) to form a buried diffusion plate (5) in the substrate involves the use of an arsenic silicate glass (ASG) film (2) (col. 5, line 18 thru col. 7, line 51). Wong et al. in view of Shen do not disclose the mask layer comprises a photoresist layer, wherein the mask layer comprises a sacrificial layer underlying the photoresist layer.

Gonzalez discloses Wong et al. disclose a method for fabricating a capacitor where a mask layer comprises a sacrificial layer underlying the photoresist layer (col. 5, lines 35-60).

Since Wong et al. and Gonzalez are both from the same field of endeavor, a method for fabricating a capacitor, the purpose disclosed by Gonzalez would have been recognized in the pertinent art of Wong et al. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Wong et al. by a mask layer comprises a sacrificial layer underlying the photoresist layer as taught by Gonzalez for definition of isolated capacitor storage nodes (col. 5, lines 55-60).

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wong et al. in view of Shen and Gonzalez as applied to claims 6 and 7 above, and further in view of Wu et al. (6,391,706).

Wong et al. disclose a method for fabricating a trench capacitor where a silicon substrate is etched to form a deep trench (1); doping the deep trench (1) to form a buried diffusion plate (5) in the substrate at a lower portion of the deep trench (1); lining the deep trench with a node dielectric layer (6); performing a first polysilicon deposition and recess etching to embed a first polysilicon (Poly1) layer (7) on the node dielectric layer (6) at the lower portion of the deep trench (1), and the Poly1 layer (7) having a top surface, wherein the top surface of the first polysilicon layer (7) and sidewall of the deep trench (1) define a first recess; forming a collar oxide layer (8) on sidewall of the first recess; performing a second polysilicon deposition and recess etching to embed a second polysilicon (Poly2) layer (11) on the Poly1 layer (7); forming

a mask layer partially masking the collar oxide layer (8); removing the collar oxide layer (8) not masked by the mask layer and the Poly2 layer (11); removing the mask layer (Fig. 13-14; col. 6, lines 41-55); and performing a third polysilicon deposition and recess etching to embed a third polysilicon (Poly3) layer (14) on the Poly2 layer (11). Wong et al. further disclose doping the deep trench (1) to form a buried diffusion plate (5) in the substrate involves the use of an arsenic silicate glass (ASG) film (2) (col. 5, line 18 thru col. 7, line 51). Wong et al. in view of Shen and Gonzalez do not disclose a sacrificial layer is made of anti-reflection coating materials.

Wu et al. disclose a method for fabricating a trench capacitor where a mask layer comprises a photoresist layer, wherein the mask layer comprises a sacrificial layer underlying the photoresist layer. Wu et al. also disclose the sacrificial layer is made of anti-reflection coating materials (col. 5, lines 51-62).

Since Wong et al. and Wu et al. are both from the same field of endeavor, a method for fabricating a trench capacitor, the purpose disclosed by Wu et al. would have been recognized in the pertinent art of Wong et al. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Wong et al. by the sacrificial layer is made of anti-reflection coating materials as taught by Wu et al. to minimize reflections and improve photoresist image fidelity (col. 5, lines 54-57).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Furukawa et al. (6,225,158) disclose a method for fabricating a trench capacitor where a pad layer is formed on a silicon substrate; etching the pad layer and the silicon substrate to form a deep trench; doping the deep trench to form a buried diffusion plate in the substrate at a lower portion of the deep trench; lining the deep trench with a node dielectric layer; performing a first polysilicon deposition and recess etching to embed a first polysilicon (Poly1) layer on the node dielectric layer at the lower portion of the deep trench, and the Poly1 layer having a top surface, wherein said top surface of the first polysilicon layer and sidewall of the deep trench define a first recess; forming a collar oxide layer on sidewall of the first recess; performing a second polysilicon deposition and recess etching to embed a second polysilicon (Poly2) layer on the Poly1 layer; and performing a third polysilicon deposition and recess etching to embed a third polysilicon (Poly3) layer on the Poly2 layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

PEP